ACCELERATING DATA SCIENCE AT THE EDGE USING FPGAS

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ABSTRACT: Data Science has matured over the past few years with novel applications in diverse areas including health, energy, autonomous x, etc. Many of these are cyber physical social systems with strict requirements of latency, throughput and energy efficiency. With recent dramatic advances in FPGAs, these devices are being used along with multi-core and emerging memory technologies to realize advanced platforms to accelerate variety of complex applications. This talk will review our work in the Data Science Lab at USC (dslab.usc.edu) and the promise of reconfigurable computing (fpga.usc.edu) leading up to current trends in accelerators for data science. We will illustrate FPGA-based parallel architectures and algorithms for a variety of data analytics kernels in streaming graph processing and machine learning for "edge" processing. While demonstrating algorithm-architecture co-design methodology to realize high performance accelerators for graphs and ML, we demonstrate the role of modeling and algorithmic optimizations to develop highly efficient IP cores. For graph embedding, we develop a novel computationally efficient technique using graph sampling and demonstrate scalable performance. For CNN inferencing, we develop parallel frequency domain convolution algorithms and data layouts to realize high throughput and energy efficient designs using FPGAs. We conclude by identifying opportunities and challenges in exploiting emerging heterogeneous architectures composed of multi-core processors, FPGAs, GPUs and coherent memory.

BIOGRAPHY: Viktor K. Prasanna is Charles Lee Powell Chair in Engineering in the Ming Hsieh Department of Electrical Engineering and Professor of Computer Science at the University of Southern California. He is the director of the Center for Energy Informatics at USC and leads the FPGA (fpga.usc.edu) and Data Science Labs (dslab.usc.edu). His research interests include parallel and distributed computing, accelerator design, reconfigurable architectures and algorithms and high performance computing. He served as the Editor-in-Chief of the IEEE Transactions on Computers during 2003-06 and is currently the Editor-in-Chief of the Journal of Parallel and Distributed Computing. Prasanna was the founding Chair of the IEEE Computer Society Technical Committee on Parallel Processing. He is hthe Steering Co-chair of the IEEE International Parallel and Distributed Processing Symposium (www.ipdps.org) and the Steering Chair of the IEEE International Conference on High Performance Computing (www.hipc.org). His work has received best paper awards at leading forums in parallel computing, HPC and FPGAs, including Computing Frontiers, International Parallel and Distributed Processing Symposium, ACM International Symposium on FPGAs, among others. He is a Fellow of the IEEE, the ACM and the American Association for Advancement of Science (AAAS). He is a recipient of 2009 Outstanding Engineering Alumnus Award from the Pennsylvania State University. He received the 2015 W. Wallace McDowell award from the IEEE Computer Society for his contributions to reconfigurable computing.