A fast and low computation consumption model for system-level thermal management in 3D IC

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***Abstract*—With the rapid increment of the power density and the introduction of vertical stack, heat dissipation has become a challenge issue. Thermal-aware placement thereby attracts more and more attentions for 3D IC. Meanwhile, as the keep-going scaling-down of IC, a huge computation consumption was caused by the large scale span. In this paper, an equivalent anisotropic thermal conductivity model was introduced to low down the computation consumption caused by the huge feature size difference. Correctness of this model was verified and the deviation from a full-scale simulation was less than 20%. By applying this model, thermal distribution of a designed 3D IC with 1566 TSVs and 80504 hot-spots was obtained with the total computation time of about 24 minutes in a regular personal computer.**

Keywords-thermal management; 3D IC; low computation

I. INTRODUCTION *(HEADING 1)*

Thermal is always a critical issue in integrated circuit (IC). [1-3] Excessive high temperature will significantly degrade the reliability of device and interconnection by decreasing the carrier mobility, causing electro-migration and other thermo-electro-mechanical coupling effects. Recently, 3D integration is receiving great interest as an alternative promising solution to keep IC staying in pace with system demands on scaling, performance and function. [4] For example, the existing 3D stacked IC products from Samsung [5] and Tezzaron [6]. Along with the higher integration degree by stacking chips vertically, severer thermal problem appears because of low thermal conductivity of interlayer dielectric and heat accumulates layer by layer as well. [7] Therefore, thermal management needs even more careful consideration in the 3D IC.

Due to high complexity of thermal analysis and high difficult in measurement of 3D IC, extensive research on simplified method is widely studied. Simplified calculation of a single structure such as TSV (Through Silicon Via) and interconnection were proposed by some researches. Detail thermal equivalent of TSV was proposed with thermal resistance network model [8]. Detail 3-D thermal circuit RC transmission line model for transient thermal analysis of interconnect structure was studied [9-10]. Via thermal effect was also consider in the paper since its high conductivity compared with other materials in ILD layers [11]. To the system level thermal calculation, 1D and 3D thermal resistance modeling are proposed to simplified thermal calculation.[12-13] Among them, EDA evaluation is a popular method that analogy the real structure into electrical resistance network and calculate with the existing software for electrical analysis.[14-15] A commercial software Hotspot, using compact thermal modeling methodology for 3D IC designed combine thermal resistance network method and consideration of thermal influence of interconnects, provided an efficient computation for early design stages.[16]

In recent 3D-IC design flow, Thermal optimizations were also considered and efforts have been made at the stages of floorplanning [17-19], placement [20-21], and routing [22-24]. However, some of the TSV-aware ones made simple assumption for the thermal conductivity of TSVs, by assuming the equivalent thermal conductivity of a thermal tile was proportional to the number of the TSVs inside that tile. Part form this, real-time computation of thermal distribution, which is necessary for interactive optimization of thermal and electrical design, is difficult to realize in most papers.

In this paper, an equivalent anisotropic thermal conductivity model was introduced to realize the real-time computation of thermal distribution with detail TSV and Cu wire in redistribution layer considered. Fast calculation of temperature was realized by a new method in simplifying the thermal conductivity and simulation.

The remainder of this paper is organized as the following. Section II describes the detail 3D IC structure and the simplified method. Section III proposes a simplified 3D IC model to verify the accurate of this model. Section IV extends the accurate thermal model for large-scale designs and presents the experimental results to show the effectiveness of our TSV planning principle.

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II. SIMPLIFIED MODEL OF TYPICAL 3D IC

In this part, a detail simplified method of 3D IC structure with a new equivalent anisotropic thermal conductivity model was introduced. In order to integrate with thermal-aware 3D placement, calculation of thermal distribution should be realized automatically as the whole structure varies. That was to say, a large-scale 3D IC with complicate structure should be simplified into the coordinate array of key cells such as hotspots and TSVs. Details was shown in this part.

A. *Typical structure and dimension of 3D IC*

Nowadays, as the development of micro-nano processing technology, such as etching and deposition, TSVs are more accessible. 3D technology and applications offer a variety of benefits: span from low power consumer electronics e.g. handheld devices to high-end products such as 3D stacked memory or multi-core microprocessors. [25] In general, die stacking comes in two different stacking topologies: (1) fine grain Face-to-Face (F2F), (2) sequential Face-to-Back (F2B). Considering F2B had been applied in the world's first multi-die FPGA proposed by Xilinx [26] and hybrid memory cube announced by Micron Technology [27], coupled with better characteristics for heat dissipation compared with F2F, only F2B structure is discussed in this paper.

A typical four layer 3D IC with F2B structure was shown in Fig. 1. The detailed data refer to the dimension of Xilinx FPGA are listed in TABLE 1.

TABLE 1 PARAMETERS OF THE 3D IC MODEL

Parameter	***Value (μm)***
thickness of Si substrate	50
thickness of BEOL layer	2
Thickness of micro-bump	15
wire width in RDL	10
Wire thickness in RDL	2
TSV diameter	10

B. *Simplified model*

It is well known that because of the enormous size difference within the chip and complex material structure, as long as large amount of thermal TSVs and thermal wires in 3D IC, computation complexity increases exponentially with the computational time out of control. By divided the small size structure such as TSV, cu wire and micro-bump as a union with the basic material, through a small enough partition and accurate equivalent, the geometric size difference would be reduced to less than one order of magnitude, which resulted in a low computation consumption and a fast calculation. So compared with the original size distribution in the IC, several orders of magnitude raised in every division so that the amount of network will be much less with the calculation decrease.

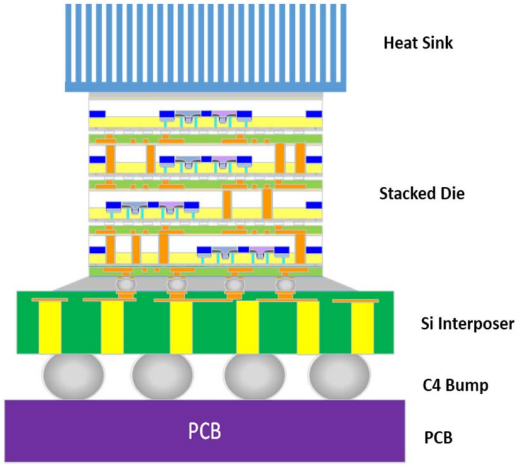


Figure 1 Typical structure of 3D IC

In z direction, because of the thermal conductivity difference existing in different layers such as Si, dielectric and underfill, every single layer was divided into four parts: Si layer, BEOL (Back End of Line) layer, wire layer and inter-layer. Among them, the Si layer, wire layer and inter-layer were mainly consist of the basic material (Si, underfill, underfill) and the inserted structure (TSV, Cu wire and micro-bump). The underfill layer was divided into 2 parts for the different proportion and location of Cu wire and micro-bump. As to the BEOL layer, since the complicate design of interconnection and high percentage of dielectric material, it was simplified as Cu via inserted into dielectric layer. The division based on thermal conductivity stratification helped raise the accurate of simplified model meanwhile reduce the calculation amount as much as possible. In x and y directions, the whole chip was divided in several parts considering the calculation ability and the calculation accuracy.

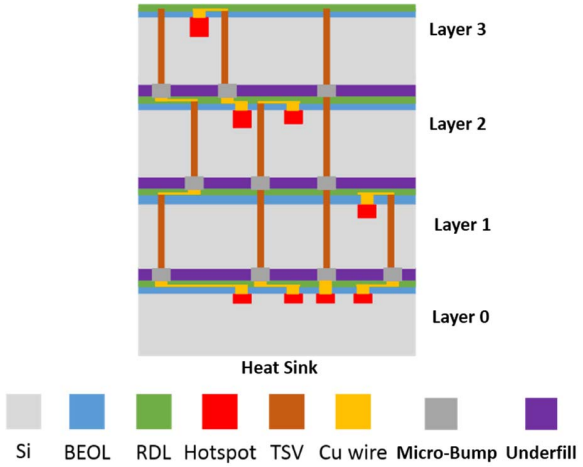


Figure 2 Simplified model of the typical structure. Hot-spots here refer to devices dissipating power. Detail information in BEOL was ignored and replaced by equivalent material. Only one-layer Cu wire in RDL was considered. The whole structure upside down for the sake of analysis with the main heat dissipation way heat sink on the bottom.

Limited by the ignorance of detail interconnection between devices in 3D IC floorplanning, only interconnection connecting with the Cu wire on RDL (Redistribution Layer) and TSV was considered in this calculation, shown as the Cu wire in Fig. 2. Hot-spots here were referred to adjacent ICs generating heat which gathering together. Hot-spots were considered located at the surface of Si substrate, that is, the active layer. Considering the ignorable thermal influence of dielectric layer of TSV, they were ignored in this paper. Dimension sizes of the structures in this paper were listed in Table 1.

III. BASIC THERMAL CONDUCTIVITY EQUIVALENT METHOD

With thermal TSVs and thermal wires in Si Substrate, underfill layer, BEOL layers and other parts of 3D IC, thermal conductivity of the 3D IC could be regarded as anisotropic, which means thermal conductivity in planar directions (x,y) k_{xy} is not the same as that in normal direction (z) k_z. With the equivalent thermal conductivities k_{xy} and k_z extracted base on the principle of thermal resistance equivalence, temperature distribution was available through COMSOL computation. Equivalent thermal conductivity of the studied block was drawn and applied in the simulation, with the specific structure in the block considered exactly.

A. *Thermo-electricity analogy method*

In the thermo-electricity analogy, temperature T is analogous to voltage U, while heat flux q to current I and thermal resistance R_{th} to electricity resistance R. Similar to the relationship among U, I and R, T is proportional to both q and R_{th} based on Fourier's law.

The most popular way to extract the equivalent thermal conductivities is based on the thermo-electricity analogy method. Shown in Fig. 3, a simple structure: Si substrate with 3 TSVs inserted was used as an example. In this figure, R represented the radius of inserted TSV; H was the height of Si substrate and TSV; A and B were respectively the length and width of Si substrate. Dielectric layer, usually made by SiO_2, was ignored in this paper.

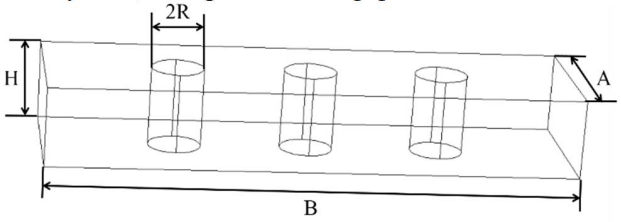


Figure 3 A simple structure constructed by a Si substrate and three TSVs inserted

Thermal diffusion was influenced by inserting of TSV, designed micro-bumps and interconnection in the chip, which meant that unlike the homogeneous material, thermal conductive in IC was anisotropic, as introduced above. Two kinds of equivalent thermal conductivities were extracted in this paper: the in-plane direction thermal conductivity k_{xy} and the cross-plane one k_z.

Take k_z as example, a uniform heat flux Q_{in} was applied on the upper side of z direction and the bottom of the block was isotherm, shown in Fig. 4. Boundary condition of other sides were set to be adiabatic. Assume that temperature on the topside were the same, namely ignore the horizontal heat flux, an equivalent resistive model was distributed in Fig. 5. The three TSVs and Si substrate, acting as four parallel thermal path, were equivalent to four parallel thermal resistance.

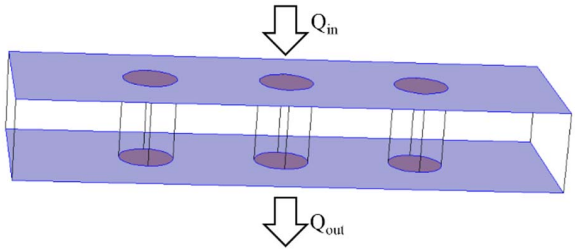


Figure 4 Structure for k_z extraction, with boundary conditions: heat flux Q_{in} applied on the top side, isothermal on the bottom side, adiabatic on the other sides.

In this case,

$$k_z = \frac{(S_{TSV} \times k_{Cu} + (S - S_{TSV}) \times k_{Si})}{S} \quad (1)$$

In (1), $S=A*B$ and $S_{TSV}=N*pi*R^2$ were defined as the horizontal cross-sectional area of Si substrate and TSV. N is the number of TSV.

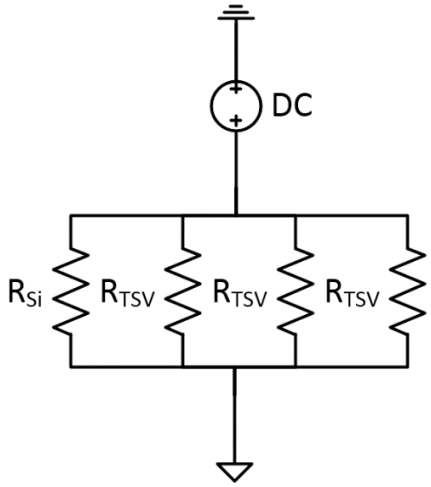


Figure 5 Equivalent resistance network

Equivalent of k_{xy} can be obtained in a similar plan.

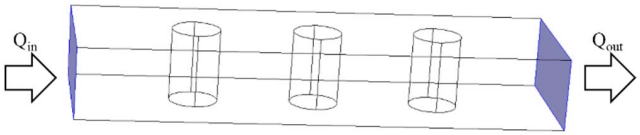


Figure 6 Structure for kxy extraction, with boundary conditions: heat flux Qin applied on the left side, isothermal on the right side, adiabatic on the other sides.

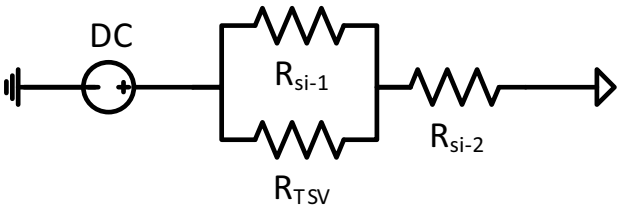


Figure 7 Equivalent resistance network

Unlike the equivalent resistance network for cross-plane thermal diffusion, structure distribution in the in-plane direction was really complexity. A simplification by taking all conductive structure as a union is made. The equivalent resistance network was shown in Fig. 7.

In this case,

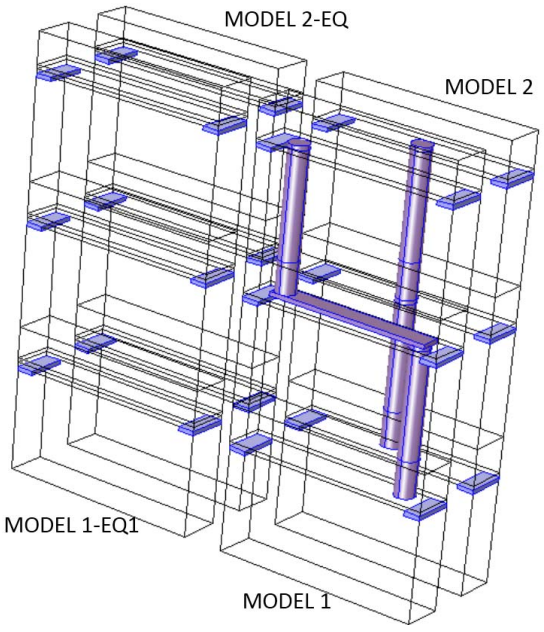
$$k_{xy} = \frac{B \times k_{xy-m} \times k_{Si}}{b \times k_{Si} + (B-b) k_{xy-m}} \tag{2}$$

$$k_{xy-m} = \frac{a \times k_{Cu} + (A-a) \times k_{Si}}{A} \tag{3}$$

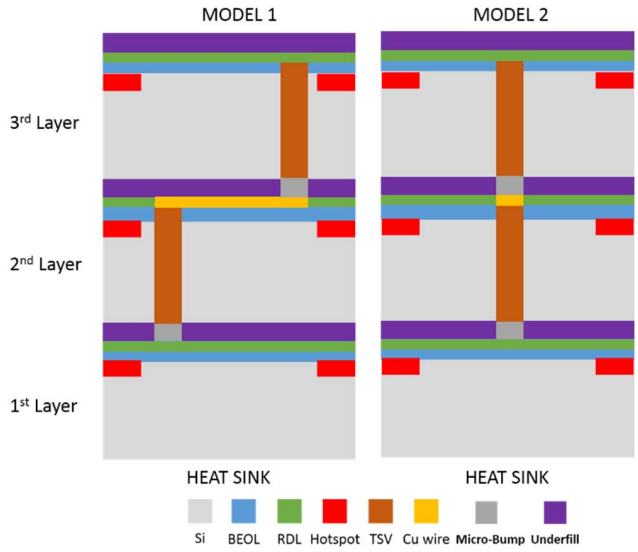
$$a = b = \sqrt{N \times \pi \times R^2} \tag{4}$$

Meaning of parameters were shown above, as k_z equivalent case.

Two three layer stacked structures with a single block on each layer were used in this paper to verify the accurate of simplified method, shown in Fig. 8. Two hot-spots were distributed on two sides of each layer. Two interconnected TSVs were inserted in the 2nd and 3rd layer. Difference between the two models was the relative distance between two TSVs. Here only the 2nd layer in model 1 was taken into example, showing the equivalent of thermal conductivities. Results were listed in Table 2.



(a)



(b)

Figure 8 Two three layer stacked structures for verification. (a) the stereogram of two models and the equivalent of two models; (b) cross-section of two models.

Simulation results were shown in Fig. 9. Two black line in the figure was the temperature distribution in model 1 and model 2 while the two red ones are the equivalent results. Two problems were illustrated from the comparison of black and red curves. The first was that the equivalent thermal conductivity was overestimated since the calculated temperature was lower the real model in the figure. The second and most important was that an opposite trend was shown in temperature calculation since temperature in model 2 was slightly higher than that in model 1.

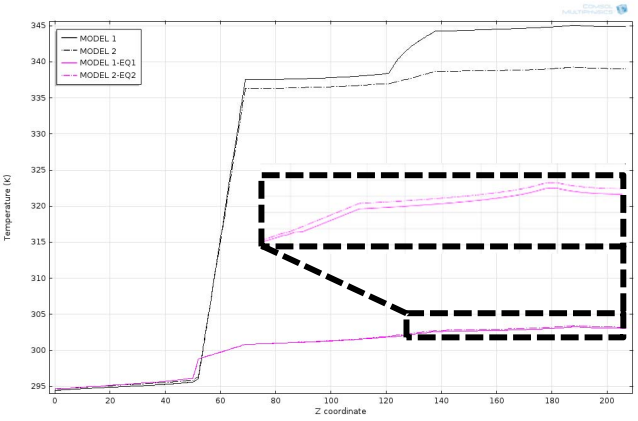


Figure 9 Simulation results of the models.

Two improvements were made to increase the accuracy of the simplified model.

B. *Thermal dissipation effective of TSV and Cu wire*

Firstly, heat flow from the upper layer was also worth noting. It was also ignored by the simplified method above.

Simulation results of the equivalent model displayed a contrary tendency just because the longer Cu wire, the better thermal property the structure was. Apparently it was wrong. To the case without TSV connection beneath, the wire length was much longer than thermal diffusion length, and thermal effect would diminish. To the case with TSV connected, obviously that shorter length induced to better thermal property since TSV helped introduce thermal through the low conductivity material and then to the next layer. And the equivalent above are all based on uniform heat flux, which was not practical because heat flux at the interface of two blocks was decided by the interconnection between them. A simple structure, shown in Fig. 10, was introduced in this paper to investigate the length of Cu wire and temperature. By simulation, relationship between wire length *l* and temperature *T* obtained.

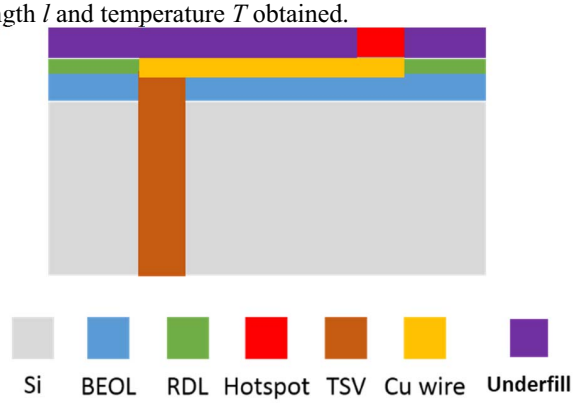


Figure 10 Simple structure constructed with a micro-bump hotspot, a Cu wire and a TSV. Used to obtain relationship between temperature and wire length.

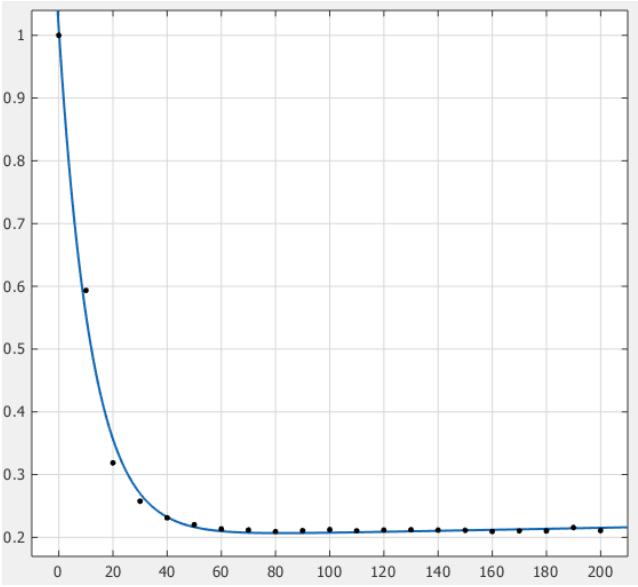


Figure 11 Normalization processing of 1/T and wire length

A coefficient *w* was proposed in this paper to describe the relationship between thermal property and wire length. *w* obtained by Normalization processing of *1/T* and wire length.

$$w = 0.8e^{-0.083\times l} + 0.2e^{0.00038\times l} \tag{5}$$

C. *Modified thermal conductivity equivalent*

Even with uniform power distribution on the top side of a block, temperature distribution in-plane would never be same, because different thermal conductivities resulted in different heat flux in-plane. Even with high thermal conductivity, only small proportion of heat flux flow through TSV and Cu wire because of their low area percentage in-plane. Optimized proportion of high conductivity material such as TSVs, Cu wires and micro-bumps need to be reduced.

Based on the above consideration, the improvement was proposed in k_z equivalent.

In the top layer with no heat flux from other layer, the coefficient *w* should not be considered.

$$k_{z-m} = \frac{(S_{TSV}\times k_{Cu} + (S - S_{TSV})\times k_{Si})}{S} \tag{6}$$

$$k_z = \frac{(S_{TSV}\times k_{z-m} + (S - S_{TSV})\times k_{Si})}{S} \tag{5}$$

While in the other layers, the coefficient *w* is added.

$$k_{z-m} = \frac{(S\times k_{Cu} + (S - S_{TSV})\times k_{Si})}{S} \tag{8}$$

$$k_z = \frac{(10\times S\times k_{z-m}\times \frac{\Sigma w}{N} + (S - S_{TSV})\times k_{Si})}{S} \tag{9}$$

Base on the improved simplified method, simulation result were obtained and shown in Fig. 12. Same as in Fig. 11, two black lines were referred to the temperature distribution in model 1 and model 2 while the red and ones were the equivalent results. Two problems illustrated in Fig. 11 were both solved. About 20 percent temperature deviation existed between the equivalent model and the real model. And the most important, the same temperature trend shown in the calculation of simplified model and the real model.

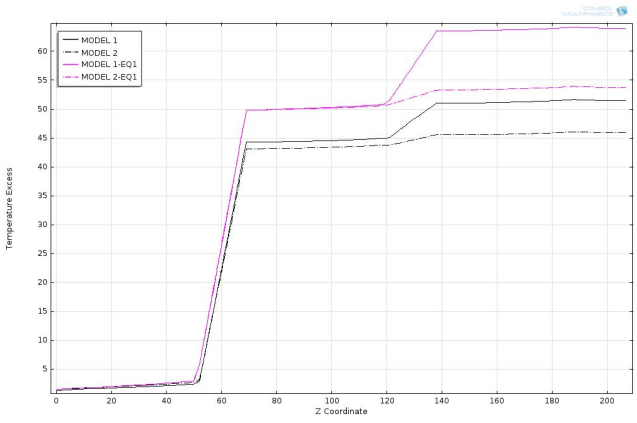


Figure 12 Simulation results of the models.

IV. EXPERIMENT RESULT

The program was written in MATLAB and run on COMSOL & MATLAB. With the equivalent thermal conductivity of each block calculated by MATLAB, the parameter was then imported in the COMSOL and assigned to the material in the model. With the structure automatically modeled in the COMSOL, temperature distribution is available after simulation.

Our method was applied in thermal floorplanning of a 3D IC based on IWLS 2005 benchmarks [28]. We synthesized the circuit with a standard cell library (gscl45nm.lef) [29] developed by Oklahoma State University and the TSV defined in .lef file. The target 3-D technology is a 4-tier 3-D IC with the 1566 TSVs and 80504 hot-spots. The power density is set on the order of magnitude of 60W/cm^2. Temperature distribution could not be simulated in a full-scale model because of the huge data and complex structure. In this paper, the chip was divided into 2560 blocks. After total computing time, about 24 minutes, temperature distribution of the processor was available. The calculation result was shown in Fig. 13.

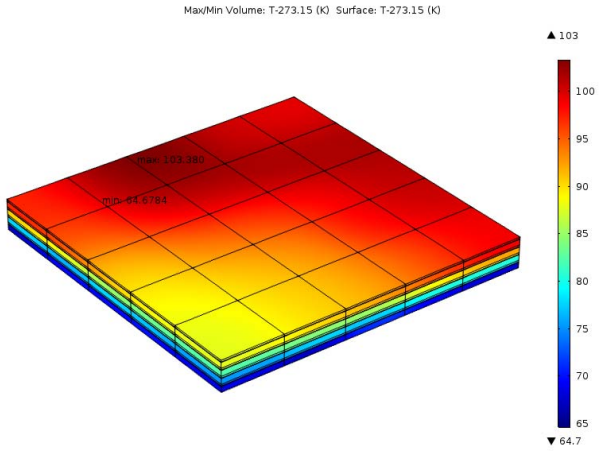


Figure 13 Simulation result with equivalent simplification.

V. CONCLUSION

An efficient method was proposed in this paper to calculate the system-level temperature distribution. Proposal of an equivalent anisotropic thermal conductivity model can greatly simplify the calculation by reducing the geometric size difference to less than one order of magnitude. Simultaneously, the accuracy of the simplification was guaranteed by introducing the modified equivalent method and the thermal wire effective coefficient which represent a consideration of heat flux distribution. Part from this, the calculation was automatically run by the pre-set program, which was necessary for interactive optimization of thermal and electrical design.

Worth mentioning that, considering repeatedly thermal computation of the whole chip was required in the validation of 3D IC partition, the present fast and low computation consumption model was the only one appropriate compared with other methods. This model was a promising way and might be widely used in system-level thermal management in 3D IC in the future.

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TABLE 2 RESPECTIVE EQUIVALENT THERMAL CONDUCTIVITIES IN MODEL 1, TAKING THE SECOND LAYER AS AN EXAMPLE

horizontal cross-sectional area of the 2nd layer in model 2	$k_{xy}=\frac{B\times k_{xy-m}\times k_{xy-basic}}{b\times k_{xy-basic}+(B-b)k_{xy-m}}$ $k_{xy-m}=\frac{a\times k_{xy-insert}+(A-a)\times k_{xy-basic}}{A}$	$k_z=\frac{(S_{insert}\times k_{z-insert}+(S-S_{insert})\times k_{z-basic})}{S}$
	$k_{xy-insert}=k_{Cu}$ $k_{xy-basic}=k_{underfill}$ $a=b=\sqrt{N\times\pi\times R^2}$	$k_{z-insert}=k_{Cu}$ $k_{z-basic}=k_{underfill}$ $S_{TSV}=N\times\pi\times R^2$
	$k_{xy-insert}=k_{Cu}$ $k_{xy-basic}=k_{underfill}$ $a=b=\sqrt{w\times l}$	$k_{z-insert}=k_{Cu}$ $k_{z-basic}=k_{underfill}$ $S_{Cu}=w\times l$
	$k_{xy-insert}=k_{Cu}$ $k_{xy-basic}=k_{SiO2}$ $a=b=\sqrt{N\times\pi\times R^2}$	$k_{z-insert}=k_{Cu}$ $k_{z-basic}=k_{SiO2}$ $S_{TSV}=N\times\pi\times R^2$
	$k_{xy-insert}=k_{Cu}$ $k_{xy-basic}=k_{Si}$ $a=b=\sqrt{N\times\pi\times R^2}$	$k_{z-insert}=k_{Cu}$ $k_{z-basic}=k_{Si}$ $S_{TSV}=N\times\pi\times R^2$