北京大学高能效计算与应用中心学术报告

Invited Talk, Center for Energy-Efficient Computing and Applications

MACHINE LEARNING ON CHIPS

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ABSTRACT: Machine learning is a powerful technique that can derive knowledge from large data set, and provide prediction and modeling. Since VLSI chip designs have extremely high complexity and gigantic data, recently there has been a surge in applying and adapting machine learning to accelerate the design closure. In this talk, we focus on some key techniques and recent developments of machine learning on chips. Three design acceleration techniques and related applications will be covered: active learning based Pareto curve learning, deep convolutional network based detection, and generative adversarial network (GAN) based design.

BIOGRAPHY: Prof. Bei Yu received his Ph.D. degree from the Department of Electrical and Computer Engineering, University of Texas at Austin in 2014. He is currently an Assistant Professor in the Department of Computer Science and Engineering, The Chinese University of Hong Kong. He has served in the editorial boards of Integration, the VLSI Journal and IET Cyber-Physical Systems: Theory & Applications. He has received four Best Paper Awards at ISPD 2017, SPIE Advanced Lithography Conference 2016, ICCAD 2013, and ASPDAC 2012, three other Best Paper Award Nominations at DAC 2014, ASPDAC 2013, ICCAD 2011, and four ICCAD/ISPD contest awards.