



INTERCONNECT AND MEMORY CHALLENGES IN INTERPOSER-BASED SYSTEMS

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ABSTRACT: Silicon interposers are already being considered for the aggressive integration of multiple 3D memory stacks in high-performance systems. This provides significant amounts of memory capacity within the package with very high bandwidths and low energy-per-bit costs. However, the full potential of all of this integrated memory may be squandered if the in-package interconnect architecture cannot keep up with the data rates provided by the multiple memory stacks. In this talk, I will first cover some of the key issues in providing the interconnect support for aggressive interposer-based memory integration. I will then present some recent research directions on how to leverage the resources of the interposer to attempt to ameliorate some of these issues, and I will also explore promising directions for additional ways to use and exploit interposers to further enhance such systems. This leads to a discussion of open problems that can provide opportunities for new research contributions from the community.

BIOGRAPHY: Gabriel H. Loh is a Fellow Design Engineer in AMD Research, the research and advanced development lab for Advanced Micro Devices, Inc. Gabe received his Ph.D. and M.S. in computer science from Yale University in 2002 and 1999, respectively, and his B.Eng. in electrical engineering from the Cooper Union in 1998. Gabe was also a tenured associate professor in the College of Computing at the Georgia Institute of Technology, a visiting researcher at Microsoft Research, and a senior researcher at Intel Corporation. He is a senior member of IEEE and distinguished scientist of the ACM, (co-)inventor on over seventy US patent applications and sixteen granted patents, and a recipient of the U.S. National Science Foundation Young Faculty CAREER Award. His interests include computer architecture, processor microarchitecture, memory systems, emerging technologies, 3D die stacking, ice hockey, snowboarding, and endurance sports.