北京大学高能效计算与应用中心学术报告

Invited Talk, Center for Energy-Efficient Computing and Applications

CROSS-LAYER OPTIMIZATIONS FOR NANOMETER VLSI IN EXTREME SCALING AND BEYOND

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ABSTRACT: As the CMOS feature enters the era of extreme scaling (14nm, 11nm and beyond), nanometer IC design and manufacturing closure challenges are exacerbated, to juggle many design metrics such as performance, power, reliability, and cost. Multiple patterning and other emerging lithography technologies have to be developed for this extreme scaling. Meanwhile, the vertical scaling with 3D-IC integration (e.g., using through-silicon-vias - TSVs) has gained tremendous interests and initial industry adoption, but TSV involves disruptive manufacturing technologies that require new modeling and design techniques for reliable 3D IC integration. Furthermore, new devices/materials such as nanophotonics are making their headways to on-chip VLSI integration for energy efficiency. All these require new design and process technology co-optimizations, which needs cross-layer modeling and abstraction. This talk will present some recent results from my research group to push the scaling envelope using emerging lithography as well as other technologies such as 3D-IC and optical interconnects. Cross-layer modeling and CAD tools/methodologies will be discussed to achieve future heterogeneous and reliable circuits and system integration.

BIOGRAPHY: David Z. Pan received his BS degree from Peking University, and MS/PhD degrees from UCLA. He was a Research Staff Member at IBM T. J. Watson Research Center from 2000 to 2003. He is currently the Engineering Foundation Professor at the Department of Electrical and Computer Engineering, UT Austin. He has published over 200 refereed journal and conference papers. He has served in many journal editorial boards (TCAD, TVLSI, TCAD-I, TCAS-II, TODAES, SCIS, JCST, etc.) and conference organizing/program committees (DAC, ICCAD, DATE, ASPDAC, ISLPED, ISPD, etc.). He is a working group member of the *International Technology Roadmap for Semiconductor* (ITRS). He has received a number of awards, including the SRC 2013 Technical Excellence Award, DAC Top 10 Author Award in Fifth Decade, DAC Prolific Author Award, 11 Best Paper Awards (ISPD 2014, ICCAD 2013, ASPDAC 2012, ISPD 2011, IBM Research Best Paper Award in CS/EE/Math 2010, ASPDAC 2010, DATE 2009, ICICDT 2009, SRC Techcon in 1998, 2007 and 2012), Communications of the ACM Research Highlights (2014), ACM/SIGDA Outstanding New Faculty Award (2005), NSF CAREER Award (2007), SRC Inventor Recognition Award three times, IBM Faculty Award four times, UCLA Engineering Distinguished Young Alumnus Award (2009), ISPD Routing Contest Awards (2007), eASIC Placement Contest Grand Prize (2009), ICCAD'12 and ICCAD'13 CAD Contest Awards, among others. He is an IEEE Fellow.