# 北京大学高能效计算与应用中心学术报告

**Invited Talk, Center for Energy-Efficient Computing and Applications**

# LOGIC OPTIMIZATION USING LOGIC IMPLICATION AND ITS APPLICATION TO VERIFICATION


## Prof. Chun-Yao Wang

**National Tsing Hua University**


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**ABSTRACT:** Node merging is a popular and effective logic restructuring technique that has recently been applied to minimize logic circuits. However, in the previous satisfiability(SAT)-based methods, the search for node mergers required trial-and-error validity checking of a potentially large set of candidate mergers. Here, we propose a new method, which directly identifies node mergers using logic implications without any SAT solving calls. To enhance the node-merging techniques on logic restructuring and optimization, we further propose a node addition and removal (NAR) approach. It works by adding a node into a circuit to replace an existing node and then removing the replaced node. We apply the node-merging and NAR approaches to circuit minimization as well as SAT-based bounded sequential equivalence checking (BSEC) to reduce the computation complexity of SAT solving.


**BIOGRAPHY:** Dr. Chun-Yao Wang received the Ph.D degree from the Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan, in 2002. His research interests include logic synthesis, optimization, and verification for VLSI/SoC designs and emerging technologies.

In 2007, Dr. Chun-Yao Wang received the Distinguished Teaching Award from the College of Electrical Engineering and Computer Science, National Tsing Hua University. In 2008, he was also awarded the Distinguished Teaching Award from National Tsing Hua University. In 2009, he was awarded the Excellent Young Electrical Engineer Medal from the Chinese Institute of Electrical Engineering. In 2011, he was a recipient of the Excellent Young Scholar Research Project from National Science Council, Taiwan.