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NEXT GENERATION ARCHITECTURE AND CAD SYSTEM FOR FPGAS

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ABSTRACT: The exploration of new architectures and CAD algorithms for large-scale FPGAs require sophisticated software that permits the modeling of the architectures, and a robust baseline CAD flow that comes close to the features and quality present in modern commercial FPGAs. This seminar will describe a set of recent advances in the open source VTR CAD flow that is a step along a path towards these goals. The flow begins with circuits captured in the Verilog language, and proceeds through elaboration, logic synthesis, physical design and timing analysis. There are three core tools: ODIN II for Verilog Elaboration and front-end hard-block synthesis, ABC for logic synthesis, and VPR [for physical synthesis and analysis. There is an associate release, version 7.0 of VTR, which has the following new features: first, the ability to support (in elaboration, physical optimization and analysis) multiple clocks in a design, and supports the industry standard SDC constraints to specify clock requirements. Second, the flow now supports hard fixed carry chains providing significant improvement in the performance of arithmetic circuits. This feature requires significant algorithmic and engineering changes throughout the flow, and enables a broad class of similar chain-like structures. Third, we introduce an energy model that permits the precise modeling of power consumption of the newer complex logic blocks, and coarse modeling of hard heterogeneous blocks. Fourth, this release provides more sophisticated packing algorithms, that are much faster than the previous release. Fifth, we describe and provide a set of FPGA architectures, and associated architecture description files. These form a basic set of architectures that can be used as is, or as the basis for enhancements. As FPGAs have become more complex, these architecture files themselves are a form of software. Sixth, we have added a feature to output a netlist describing the details of the final routed circuit that will be useful in downstream research seeking accurate timing, energy and the ability to model defects. Finally, we provide a set of measurements of the quality of results of this release and compare it to the set of prior major releases. This work is a world-wide collaboration among several contributing Universities and companies.

BIOGRAPHY: Jonathan Rose is a Professor in the Edward S. Rogers Sr. Department of Electrical and Computer Engineering at the University of Toronto. He received the Ph.D. degree in Electrical Engineering in 1986 from the University of Toronto. From 1986 to 1989, he was a Post-Doctoral Scholar and then Research Associate in the Computer Systems Laboratory at Stanford University. In 1989, he joined the faculty of the University of Toronto. He spent the 1995-1996 year as a Senior Research Scientist at Xilinx, in San Jose, CA, working on the Virtex FPGA architecture. From 1989 until 1999 he was an NSERC University Research Fellow.

He served as Chair of the Edward S. Rogers Sr. Department of Electrical and Computer Engineering from January 2004 through June 2009.

He was a visiting Professor at Imperial College, in London, in the Fall of 2009, and at the University of California, Berkeley in February, 2010. In May of 2011 he was a visiting Professor at Addis Ababa University in Ethiopia.

He is a Senior Fellow of Massey College in the University of Toronto, a Fellow of the IEEE, a Fellow of the ACM, a Fellow of the Canadian Academy of Engineering, a Fellow of the Royal Society of Canada, and a Foreign Associate of the American National Academy of Engineering.

His research covers all aspects of FPGAs including their architecture, Computer-Aided Design (CAD), Field-Programmable Systems, Soft Processors, vision and bioinformatic applications of programmable hardware