北京大学高能效计算与应用中心学术报告

Invited Talk, Center for Energy-Efficient Computing and Applications

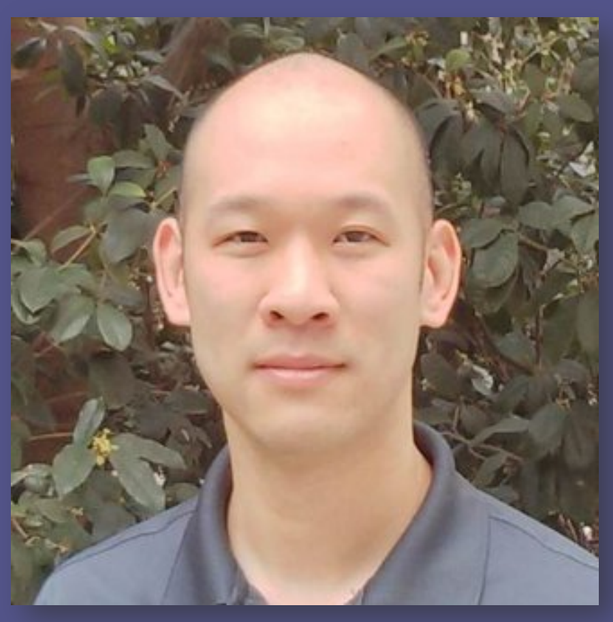
ARCHITECTING COMPUTER SYSTEMS FOR THE DIE-STACKING FUTURE

Dr. Gabriel Loh

Advanced Micro Devices

2012年4月26日　星期五　02:00pm

理科二号楼2736报告厅



ABSTRACT: Three-dimensional die-stacking technologies are rapidly maturing, with intense research and development happening in the areas of manufacturing, EDA/CAD, test and yield improvement. Stacking DRAM with high-performance computing (e.g., multi-core CPUs, heterogeneous APUs) potentially provides benefits in terms of reduced memory latency, increased memory bandwidth, and reduced memory power. To achieve the full potential of stacked DRAM, however, the stacked DRAM cannot be simply interfaced using traditional organizations. In this talk, I will focus on possible directions for using stacked DRAM and the associated challenges, opportunities, and some possible solutions. The talk will also cover other research problems related to die-stacked computer architectures beyond DRAM-stacking issues.

BIOGRAPHY: Gabriel Loh is a Principal Researcher at Advanced Micro Devices (AMD). Gabe received his PhD and MS in computer science from Yale University and his BE in electrical engineering from the Cooper Union. Gabe was also a tenured associate professor in the College of Computing at the Georgia Institute of Technology, a visiting researcher at Microsoft Research, and a senior researcher at Intel Corporation. His research interests include computer architecture, processor microarchitecture, emerging technologies and 3D die stacking. He is a senior member of IEEE and the ACM.